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MOSCONE WEST CENTER
SAN FRANCISCO, CA, USA



SIEMENS

A New Frontier for Floorplanning with AI

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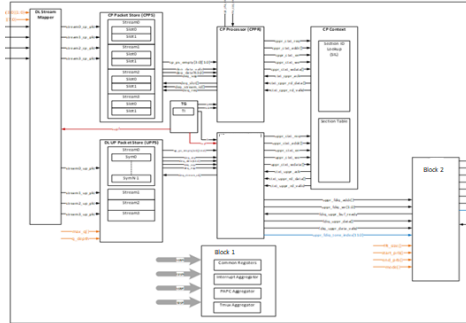
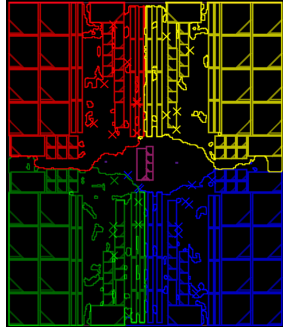
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Motivation

Macro Placement for 5G Datapath Designs



Maxlinear designs have repeated structures (same design instantiated multiple times)

Memories are instantiated at different hierarchies and **repeated 4 times** for better throughput. Datapath **latency requirement** is very tight **~210 μ s for de-jitter** with existing memories

High data storage requirement of 13760 bytes, and each memory physical dimension is **3424 deep x (128 + 9 ecc) 137 bit wide**

Memories interact to other memories with high datapath depth, adding placement and performance complexity

Due to these complexities, macro placement currently requires experienced physical designers with direct design expertise

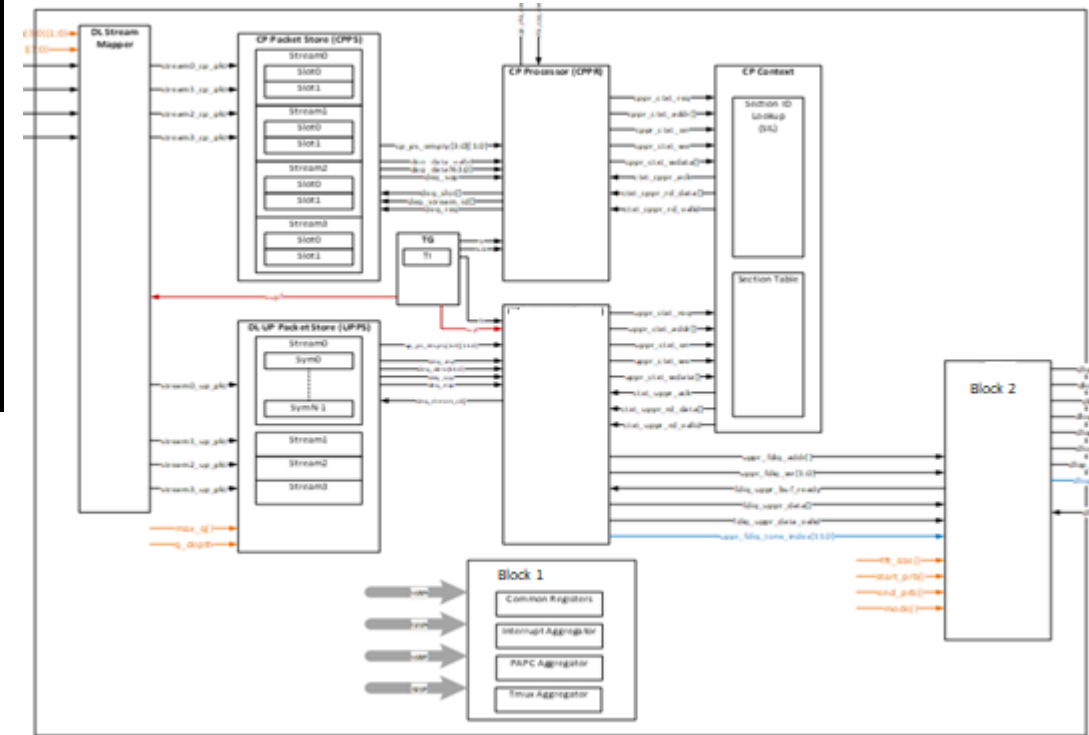
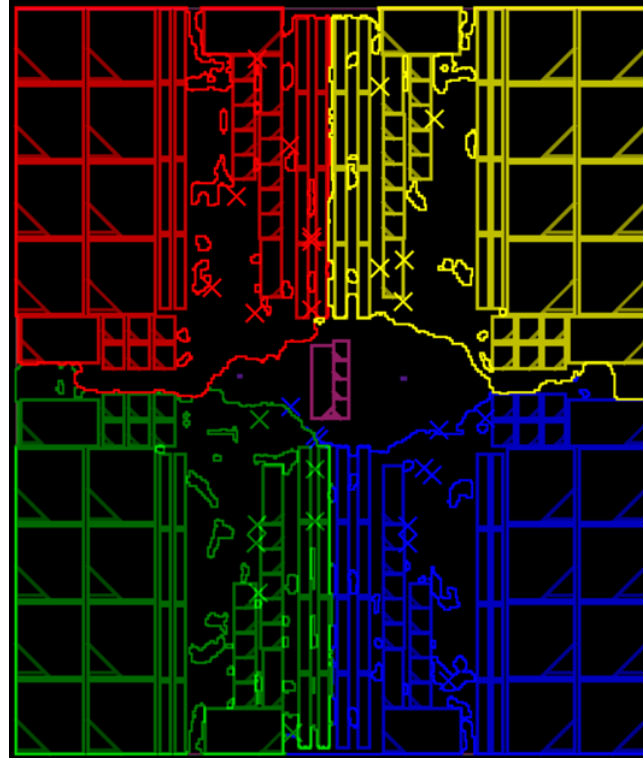
Iterative full-flow process takes weeks and even months, to confirm optimal location of the macros for best performance and routability

Handcrafted flow, results in unintended creation of uneven placement areas, which cause:

- Difficulty meeting clocking and latency targets
- Difficulty meeting IR/EM requirements

Design Specifications

- Technology : 16FFC
- Block Size : 1450um x 2100um
- Std cells : 2M+
- Memories : ~250
- Frequency : 450+
- Logic Depth : ~70 levels
- Datapath latency requirement : ~210 μ s for de jitter with existing memories



Exploring an Automated Methodology

Considerations

Automated way to place the macros without user guidance

Concentration efforts on timing, congestion and logical connectivity of various hierarchies

Fast runtimes to iterate with various floorplan sizes and metric weights

Various macro placement suggestions to select right outcome as per top-level needs

Availability of easy-to-use editing tools to refine the macro locations to utilize prior expertise

Through these considerations Maxlinear decided to look into Aprisa's AI-driven Auto Macro Placement technology

Aprisa Auto Macro Placement (AMP)

Why AI on a Macro Placer?

Learn

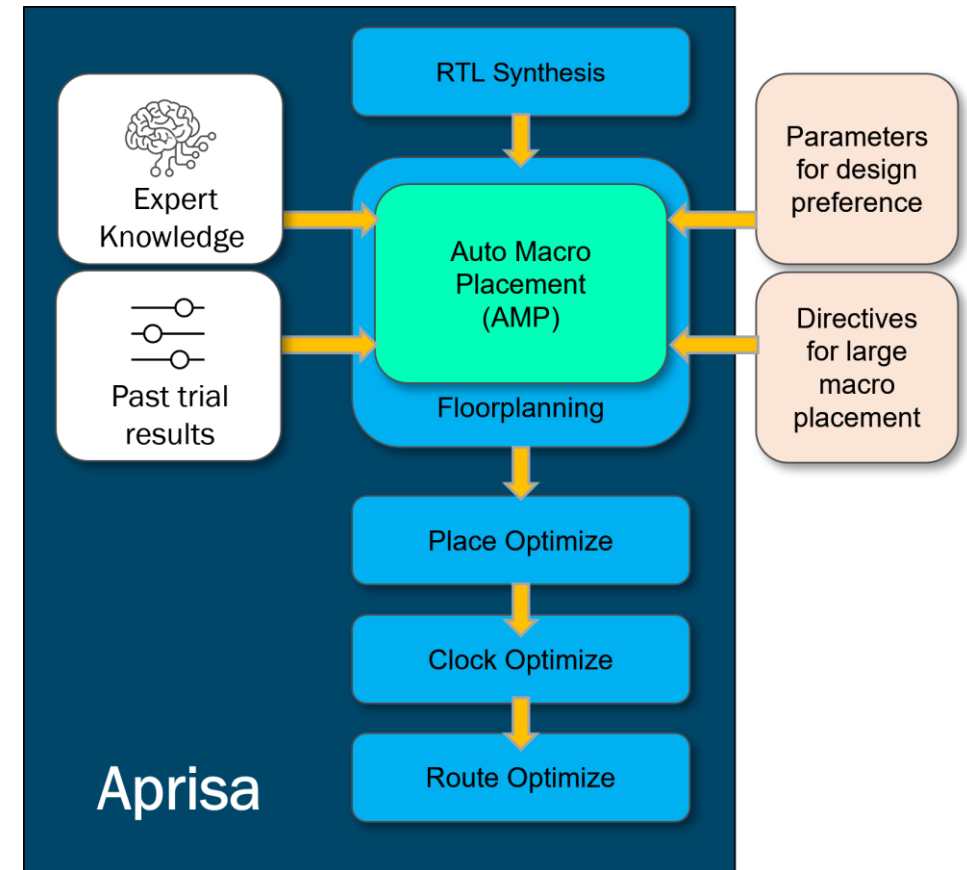
- Inference of complex data flow and handling larger number of macros
- Account for metrics that human experts cannot do without full P&R iterations to confirm results, such as accounting for IR/EM, jitter, congestion, and PPA

Train

- The solution must match or surpass design expert handcrafted results
- The algorithm must weigh in different input metrics, and analyze continuously and on the fly the best floorplan options to meet those metrics

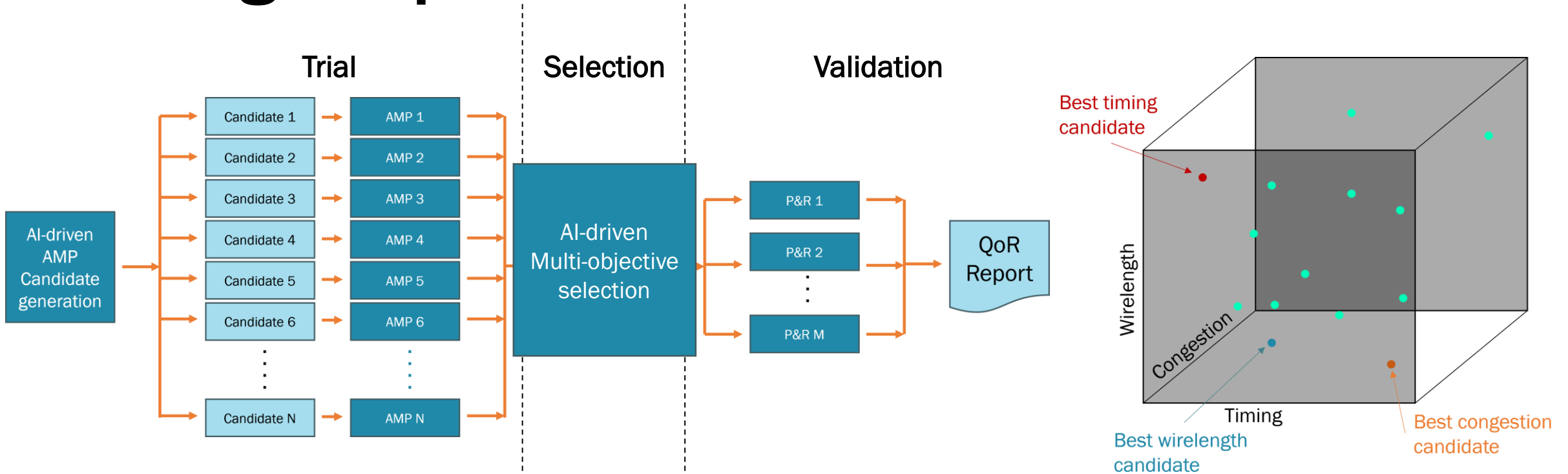
Deploy

- The algorithm must determine an option that can be measured accurately at the placement optimization step, and carry those results through to tapeout
- Parametric inputs from the user to guide the algorithm



- Congestion-driven and timing-driven engine
- Built-in expert knowledge and best practices
- Design preference and directives driven by users

AI Design Exploration with AMP



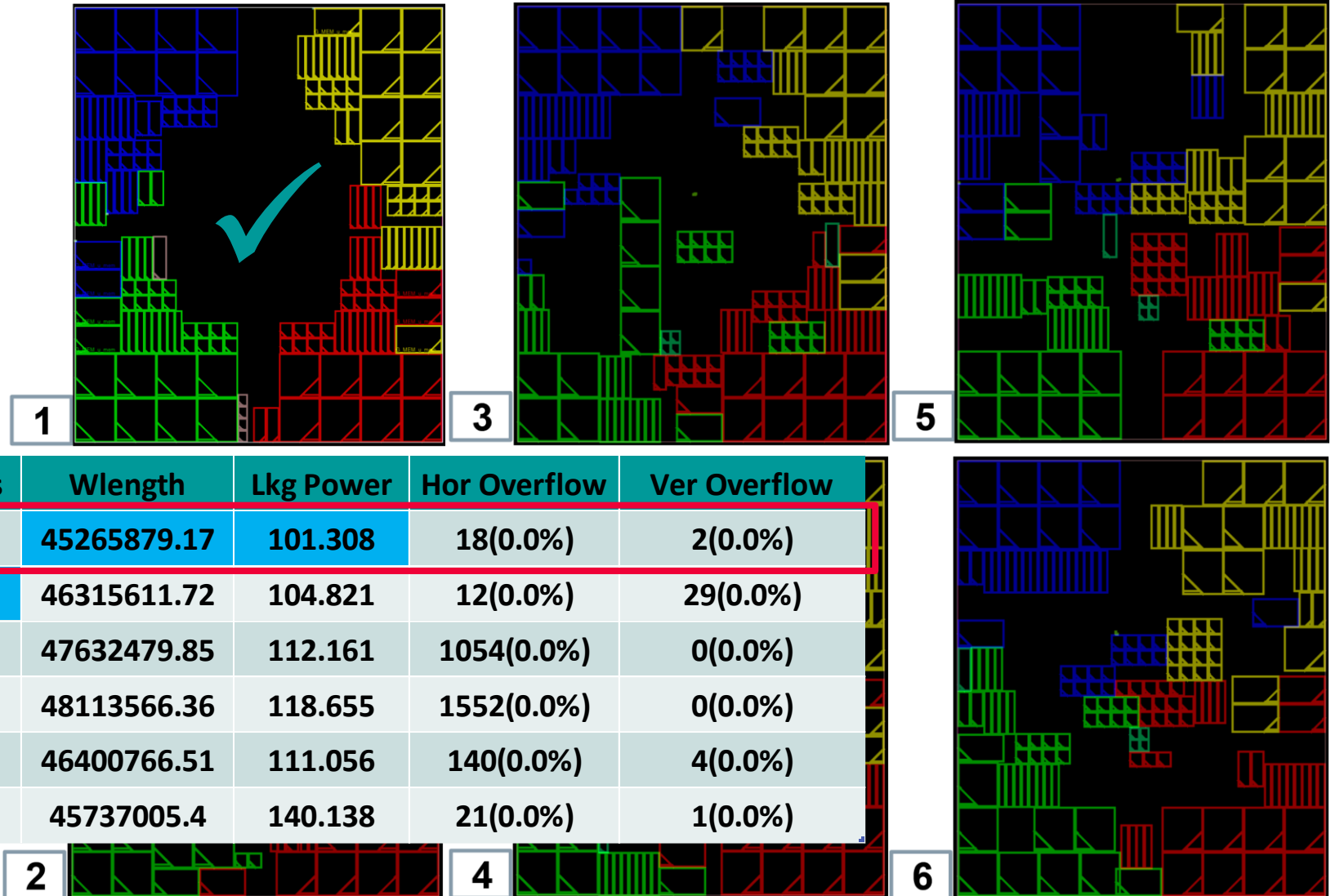
Bayesian Design Exploration

- Select best macro placement candidates based on multiple design objects
 - Timing, Wirelength, Congestion
- Carry through P&R flows to validate final QoR

AI-driven multi-objective selection algorithm, finds the best candidates for each desired metrics so a candidate can be selected according to the tradeoffs that matter most to the project

Methodology Implementation

- AMP trial ran 6 parallel options with a runtime of 2 hours



| FP | WNS(ns) | TNS(ns) | Area | Instances | Wlength | Lkg Power | Hor Overflow | Ver Overflow |
|----|---------|---------|--------|-----------|-------------|-----------|--------------|--------------|
| 1 | -0.038 | -0.963 | 743300 | 1819245 | 45265879.17 | 101.308 | 18(0.0%) | 2(0.0%) |
| 2 | -0.049 | -1.437 | 743800 | 1818322 | 46315611.72 | 104.821 | 12(0.0%) | 29(0.0%) |
| 3 | -0.004 | -0.041 | 745800 | 1823313 | 47632479.85 | 112.161 | 1054(0.0%) | 0(0.0%) |
| 4 | -0.034 | -1.235 | 749500 | 1833785 | 48113566.36 | 118.655 | 1552(0.0%) | 0(0.0%) |
| 5 | -0.006 | -0.086 | 747000 | 1827634 | 46400766.51 | 111.056 | 140(0.0%) | 4(0.0%) |
| 6 | -0.127 | -14.523 | 744500 | 1822967 | 45737005.4 | 140.138 | 21(0.0%) | 1(0.0%) |

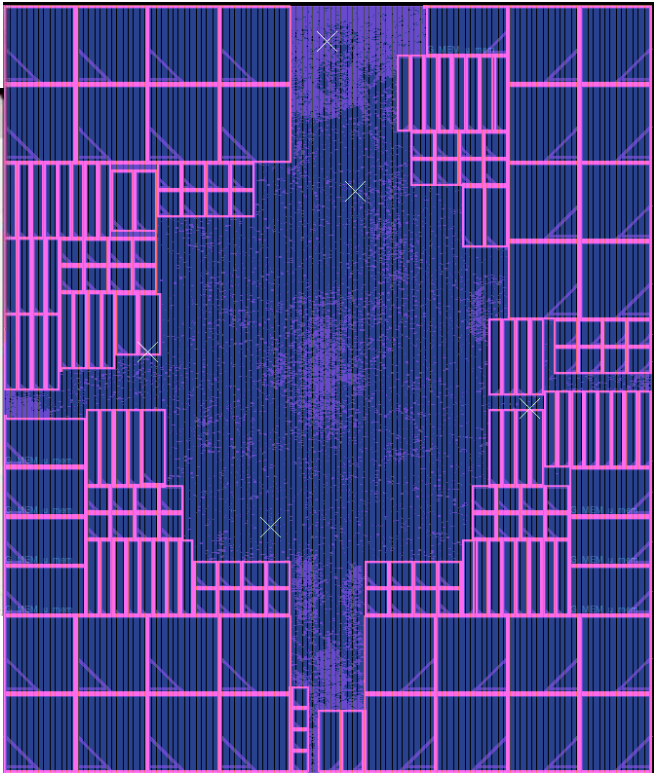
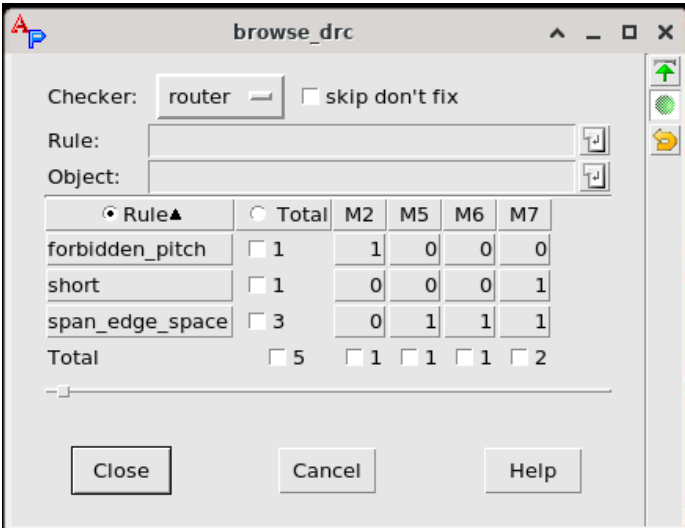
Aprisa AMP vs. Tapeout Results

- Maxlinear chose floorplan (#1) for full P&R flow and signoff, and for performance checks and physical verification
- **Aprisa AMP's implemented design met performance and DRC metrics, similar to reference handcrafted flow**
- Full P&R flow in Aprisa took 1 week to complete, producing a routable design
 - For comparison, the handcrafted method required an expert physical design engineer to spend several weeks to identify the right floorplan, and to run the full-flow for each iteration, in order to achieve the required QoR
 - Aprisa AMP, without prior input knowledge, saved the designers ~3 to 4 weeks of manual effort and time spent on closing the design

| QoR Parameter | Tapeout | AI-AMP |
|-----------------------|-----------------|------------------|
| WNS (Setup/Hold) (ns) | -0.045 / -0.033 | -0.040 / -0.020 |
| TNS (Setup/Hold) (ns) | -16.27 / -8.343 | -24.029 / -5.637 |
| # FEP (Setup/Hold) | 2544 / 5060 | 3359 / 3906 |
| # std cells | 1955777 | 1934763 |
| std-cell utilization | 45.41 % | 45.10 % |
| # DRC | 62 (10 shorts) | 97 (13 shorts) |

Signoff Timing and DRC Results

- Only a handful of DRCs encountered during DRC sign-off
- Timing checked using reference signoff tool
- Excellent timing correlation seen with the results

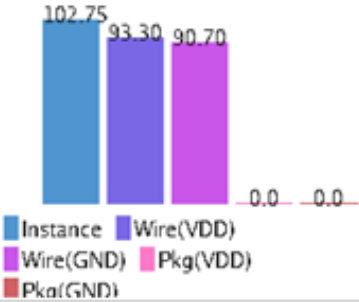


| Setup | | | Hold | | | Maxtran | | MinPeriod | | MinPulse | | Noise | |
|--------|--------|-----|--------|--------|-----|---------|-------|-----------|-----|----------|-----|--------|-----|
| WNS | TNS | FEP | WNS | TNS | FEP | WNS | FEP | WNS | FEP | WNS | FEP | Slack | FEP |
| -0.048 | -0.113 | 6 | -0.046 | -8.114 | 889 | -0.468 | 38120 | 0 | 0 | 0 | 0 | -116.5 | 38 |

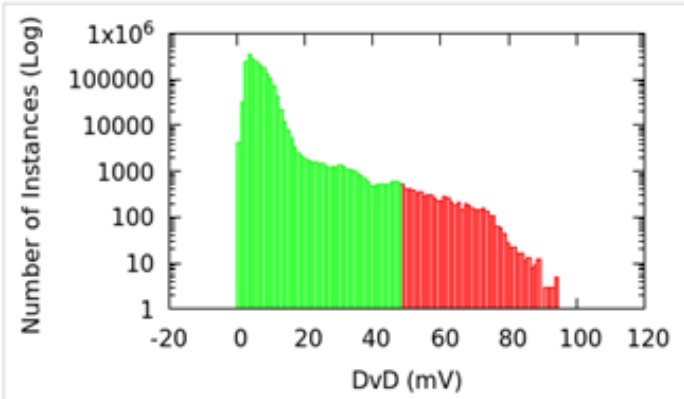
IR Sign-off Results

| Key Parameters | |
|-----------------------|--------------------------------|
| Design Name | Block |
| Design Size | 2013.6000000000001u x 2331.83u |
| Instance Count | 2226193 |
| No of Voltage domains | 1(Power) & 1(Ground) |
| Total Power | 1.581 W |
| Dominant Frequency | 492.12 MHz |
| Temperature | Details |
| Min Supply Voltage | 0.8 V |

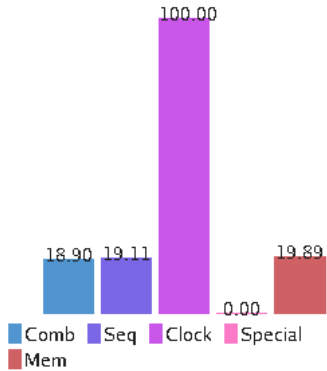
| Worst Voltage Drop Data | |
|-------------------------|---------------------|
| Parameter | Value |
| Instance | 102.75 mV (12.84 %) |
| Wire(VDD) | 93.30 mV (11.66 %) |
| Wire(GND) | 90.70 mV (11.33 %) |
| Pkg(VDD) | 0.0 mV (0.0 %) |
| Pkg(GND) | 0.0 mV (0.0 %) |



Instance Based DvD Histogram

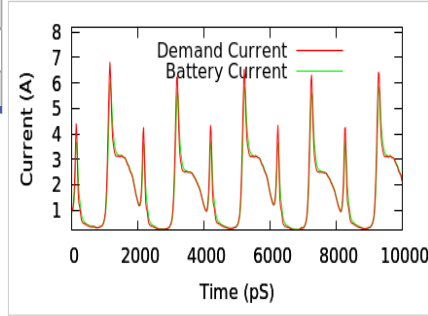


| Switching Activity | |
|--------------------|-------------------------|
| Type | Switching (%) |
| Combinational | 338812/1792374 (18.90%) |
| Sequential | 40582/212364 (19.11%) |
| Clock | 15858/15858 (100.00%) |
| Special | 0/0 (0.00%) |
| Memory/IP | 36/181 (19.89%) |
| Total | 395288/2020777 (19.56%) |



| Waveform Data | |
|-----------------|-----------------|
| Type | Peak Value (mA) |
| Battery Current | 6028.38 |
| Demand Current | 6822.47 |

Battery/Demand Current



- Few outliers were seen in IR which were known and could be fixed through the AMP flow
- IR converged with Aprisa's AMP flow, and no major issues were seen

Summary

Methodology proven to reduce floorplanning effort and time, using AI-driven macro placement technology

Aprisa AMP demonstrated that it could identify sub-hierarchies, giving it the ability to group macros to the right cluster

Aprisa AMP gave us expert quality macro placement and saved us ~3 to 4 weeks of manual effort with its AI-driven approach

Feature was tried on three additional blocks with similar findings, giving us confidence on the results

Complex designs implemented with **Aprisa AMP** can reduce overall turnaround time and help ensure time-to-market



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Thank You!

